Amendments to the Specification:

Please replace paragraphs [0005]-[0006] with the following replacement paragraphs.

[0005] Another problem with PLL spread spectrum clock generators is the resulting reduction in processing throughput of the microprocessor that is clocked by the spread spectrum clock signal. Microprocessor**s** typically have maximum allowable clock frequencies. A microprocessor may fail if the clock signal is increased beyond the maximum frequency. For many applications, it is desired to operate the microprocessor with the highest frequency clock signal possible in order to maximize microprocessor processing throughput. In order to perform the spread spectrum clock generation, however, the frequency of the clock signal is dithered between the maximum frequency and a lesser frequency. The average clock frequency is therefore lower than the maximum clock frequency. The result is an undesired reduction in microprocessor throughput.

[0006] Due to the interest in maximizing processing throughput, spread spectrum clocking of a microprocessor may be practiced by varying the frequency of the clock signal just enough to bring the peak EMI levels within the maximum permitted levels, while at the same time maintaining the fastest possible average clock frequency. Consequently, it is ~~be~~ desirable to control the variations in the frequency of the spread spectrum clock.

Please replace paragraphs [0030]-[0031] with the following replacement paragraphs.

[0030] The third and fourth bits 51-52 of spread spectrum control register 39 (the slope control bits) control the slope of control signal 60. Thus, slope control bits 51-52 also control the rate at which the frequency of output signal 38 changes. The contents of slope control bits 51-52 ~~is~~are provided to analog integrator and biasing circuit 42.

[0031] Bits five through eight 53-56 of spread spectrum control register 39 (the dither rate control bits) control the period or time duration of cycles of control signal 60. Thus dither rate control bits 53-56 also control the time it takes the frequency of output signal 38 to vary from its maximum frequency to its minimum frequency. The contents of dither rate control bits 53-56 ~~is~~are provided to counter portion 41

Please replace paragraphs [0039]-[0040] with the following replacement paragraphs.

[0039] The contents of offset control bits 49-50 in programmable spread spectrum control register 39 ~~is~~are provided to gate leads of two transistors 80-81 of analog integrator and biasing circuit 42. By turning transistors 80-81 on or off, the DC bias voltage on node 82 of voltage divider 83 can be controlled. By decreasing the bias

voltage at node 82 such that the average voltage of intermediary signal 58 decreases, the average propagation delay through variable delay element 45 is increased. By increasing the bias voltage at node 82 such that the average voltage of intermediary signal 58 increases, the average propagation delay through variable delay element 45 is decreased.

[0040] The contents of slope control bits 51-52 ~~is~~are provided to gate leads of two transistors 84-85 of analog integrator and biasing circuit 42. By turning transistors 84-85 on or off, the voltage on a node 86 is set. By setting the voltage on node 86, the current passing through current mirror 87 is set, thereby determining the slope of intermediary signal 58. By decreasing the voltage on node 86, the current passing through mirror 87 is increased, thereby increasing the slope of intermediary signal 58 and thereby increasing the rate of change of the frequency of output signal 38. By increasing the voltage on node 86, the current passing through current mirror 87 is decreased, thereby decreasing the slope of intermediary signal 58 and thereby decreasing the rate of change of the frequency of output signal 38